What is Claimed is:

1. A storage device comprising:

a nonvolatile memory; and

a control circuit,

wherein said nonvolatile memory has a plurality of a plurality of memory blocks, each of which has a plurality of sub memory blocks comprising a plurality of nonvolatile memory cells, and is capable of performing programming to a first sub memory block within a first memory block and a second sub memory block within a second memory block in parallel,

wherein said control circuit controls programming to said nonvolatile memory with an address information and data in accordance with being issued from an outside device,

wherein said first sub memory block of said first memory block includes a management area for storing a management information which includes a linking information between said first sub memory block of said first memory block and corresponding sub memory blocks of other memory blocks,

wherein said control circuit controls that reading said linking information from said first sub memory block of said first memory block in accordance with said

address information, and programming to one or more of said first sub memory block of said first memory block in accordance with said address information and corresponding sub memory blocks of other memory blocks relating to said first memory block by said linking information.

2. A storage device according to claim 1, further comprising a translation table,

wherein said translation table is used for translating from said address information issued from said outside device to a first physical address for selecting said first sub memory block of said first memory block,

wherein said control circuit reads said linking information from said first sub memory block of said first memory block selected by said first physical address translated by said translation table from said address information.

3. A storage device according to claim 2, further comprising a buffer memory,

wherein said buffer memory is capable of storing data supplied from or supplying to said outside device,

wherein said translation table is storing to said nonvolatile memory when power supplying is turned off,

and is storing to said buffer memory when power supplying is turned on.

4. A storage device according to claim 3,

wherein said nonvolatile memory cells including said sub memory blocks are coupled to a word line, and

wherein said selecting of said sub memory block is selecting said word line corresponding to said physical address.

5. A storage device according to claim 4,

wherein when said control circuit detects existing an error nonvolatile memory cell in a third sub memory block related by said linking information in said first sub memory block, said control circuit controls changing said linking information replacing said third sub memory block to a forth sub memory block.

6. A storage device according to claim 5,

wherein in said programming to said first sub memory block, said control circuit controls reading data from said first sub memory block, merging data read from said first sub memory block and new data received from said outside device and programming to a new first sub memory block, a second physical address of which is different

from said first physical address of said first sub memory block.

7. A storage device according to claim 6,

wherein said control circuit controls changing said translation table replacing said first physical address of said first sub memory block to said second physical address of said new first sub memory block as a corresponding physical address of said address information received from said outside device, after programming to said new first sub memory block.

8. A storage device according to claim 7,

wherein said management information includes a first information which indicates that each of said first sub memory block and said corresponding sub memory blocks of other memory blocks relating to said first memory block by said linking information is already erased or not.

9. A storage device according to claim 8, further comprising a plurality of volatile memories,

wherein each of said volatile memories is corresponding to each of said memory blocks and is capable of storing program data.

10. A storage device according to claim 9,

wherein in said programming to said first sub memory block, said control device controls reading data from said first sub memory block to said volatile memory corresponding to said first memory block.